29.7 ESD Protection for Mixed-Voltage I/O in Low-Voltage Thin-Oxide CMOS

Ming-Dou Ker, Wei-Jen Chang, Chang-Tzu Wang, Wen-Yi Chen

National Chiao-Tung University, Hsin-Chu, Taiwan

The thickness of gate oxide in advanced CMOS technologies has been scaled down to improve circuit operating speed. However, the I/O circuits must drive or receive high-voltage signals to communicate with other ICs in the microelectronic system. To solve the gate-oxide reliability issue without using additional thick gate oxide process [1], the stacked-NMOS configuration has been widely used in mixed-voltage I/O interfaces [1], [2]. But, stacked-NMOS often have much lower electrostatic discharge (ESD) level and slower turn-on speed, as compared with single NMOS [3]. In this work, a novel ESD protection design with a high-voltage-tolerant power-rail ESD clamp circuit is designed to protect the mixed-voltage I/O interfaces against ESD stresses in a 0.13μm 1.2V CMOS process.

The proposed ESD protection design with ESD_BUS for 1.2V/2.5V mixed-voltage I/O interfaces is shown in Fig. 29.7.1. The stacked-NMOS and pull-up PMOS (with gate-tracking circuit and n-well self-biased circuit) are the typical implementation of a mixed-voltage output buffer with only thin gate-oxide devices [2]. The ESD protection design is realized with the diodes Dp, Dn, D1, the ESD_BUS, the high-voltage-tolerant power-rail ESD clamp circuit, and the low-voltage power-rail ESD clamp circuit. The positive-to-VSS (PS-mode), negative-to-VSS (NS-mode), positive-to-VDD (PD-mode), and negative-to-VDD (ND-mode) ESD stresses on the mixed-voltage I/O pad have the corresponding ESD discharging paths in the proposed ESD protection scheme. Moreover, such ESD_BUS and the high-voltage-tolerant power-rail ESD clamp circuit can be shared with other mixed-voltage I/O pads to achieve whole-chip pin-to-pin ESD protection.

D1 is used to keep the initial voltage level of ESD_BUS at 1.2V after the chip has been powered on. When the input signals of 2.5V reach to the I/O pad, the ESD_BUS line will be charged up to 2.5V through Dp. So, the high-voltage-tolerant power-rail clamp circuit must sustain the high-voltage (2.5V) stress in this mixed-voltage I/O circuit. The low-voltage power-rail ESD clamp circuit can be realized by the traditional RC-based ESD detection circuit with 1.2V devices [4].

Figure 29.7.2 shows the high-voltage-tolerant power-rail ESD clamp circuit realized with only 1.2V devices for 2.5V mixed-voltage I/O applications, which contains the ESD clamp device and an ESD detection circuit. The ESD clamp device (Mn1 and Mn2) is realized by the stacked-NMOS (STNMOS) with the substrate-triggered technique [5]. The STNMOS is kept off without gate-oxide reliability during normal operation conditions. The ESD detection circuit is kept inactive during normal operation conditions, but it becomes active to provide substrate-triggered current to quickly trigger STNMOS on under ESD stress conditions. Here, the time constant of R2 and C (Mp3) should be designed to be on the order of ~ 1μs to distinguish the power-on transition (the supply voltage with a rise time of several milliseconds) from the ESD transition (the ESD voltage with a rise time of several nanoseconds).

In normal operation conditions with ESD_BUS of 2.5V and VDD power supply of 1.2V, Mp1 and Mp2 are kept off but Mn3 is turned on to bias the substrate of STNMOS at VSS, such that STNMOS is guaranteed to be kept off. The voltages across the gate-drain, gate-source, and gate-bulk terminals of every device do not exceed the process limitation (~1.32V in a given 1.2V CMOS process).

When an ESD transient voltage is applied to ESD_BUS with VSS relatively grounded, but VDD floating with an initial voltage level of 0V, Mp1 and Mp2, whose initial gate voltages are at a low voltage level (~0V), can be quickly turned on by ESD energy to generate the substrate-triggered current (I_{trig}) into the substrate of STNMOS. After the base-emitter voltage of the parasitic lateral n-p-n BJT in STNMOS is greater than its cut-in voltage, the STNMOS will be triggered into its snapback region to discharge ESD current from ESD_BUS to VSS. The transient simulation of the ESD detection circuit under ESD transition is shown in Fig. 29.7.3. When a 0-to-5.5V ESD-like voltage pulse with a rise time of 10ns is applied to ESD_BUS, the I_{trig} can be conducted through Mp1 and Mp2 in the ESD detection circuit to trigger STNMOS on.

The turn-on speed of STNMOS with or without ESD detection circuit is measured and shown in Fig. 29.7.4, where a 0-to-20V voltage pulse with a rise time of 10ns is applied to ESD_BUS with grounded VSS and floating VDD. The overshooting peak voltage of STNMOS without the ESD detection circuit is about 10V, which could damage the gate oxide of the low-voltage devices. In contrast, a 20V voltage pulse can be quickly clamped, by STNMOS with the ESD detection circuit, to a low voltage level without suffering the high overshooting voltage.

Transmission line pulsing (TLP) generator is used to verify the secondary breakdown current (It2) of STNMOS with or without ESD detection circuit. The measured TLP I-V curves of STNMOS with device dimension (W/L) of 240μm/0.2μm are shown in Fig. 29.7.5. The STNMOS with an ESD detection circuit can be triggered on at a lower voltage level than that without an ESD detection circuit. In addition, the turn-on uniformity among the multiple fingers of STNMOS can be improved to enhance its ESD robustness by the substrate-triggered effect [5], such that the It2 of STNMOS with the ESD detection circuit can be increased from 1.4A to 2.4A. The human-body-model (HBM) and machine-model (MM) ESD level of STNMOS devices with different device dimensions are shown in Fig. 29.7.6. With the substrate-triggered current generated from the ESD detection circuit, the turn-on uniformity of STNMOS can be effectively improved to achieve a higher ESD robustness

The R_{ESD} in Fig. 29.7.1 should be designed a little larger than some critical value (~10Ω), such that STNMOS in the mixed-voltage I/O interface will not be damaged before the ESD current is discharging through the diode Dp, ESD_BUS, and the high-voltage-tolerant power-rail ESD clamp circuit to the grounded VSS under the PS-mode ESD stress.

A novel ESD protection design for 1.2V/2.5V mixed-voltage I/O interfaces by using high-voltage-tolerant power-rail ESD clamp circuit realized with low-voltage devices has been successfully verified in a 0.13μm CMOS process. The four-mode (PS, NS, PD, and ND) ESD stresses on the mixed-voltage I/O pad and pin-to-pin ESD stresses can be effectively discharged by the proposed ESD protection scheme.

References:

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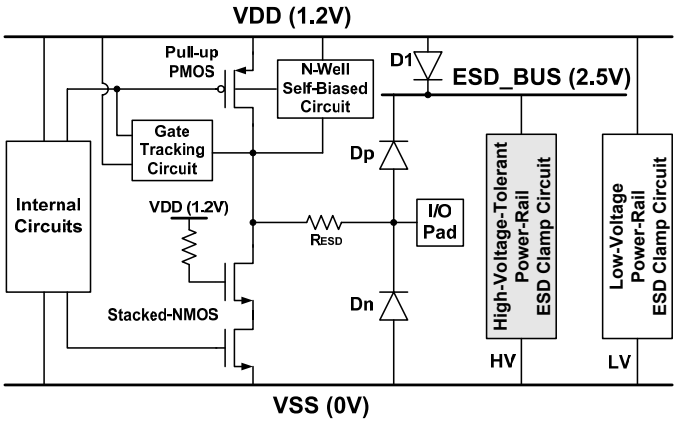


Figure 29.7.1: ESD protection scheme for mixed-voltage I/O interfaces with the high-voltage-tolerant power-rail ESD clamp circuit.

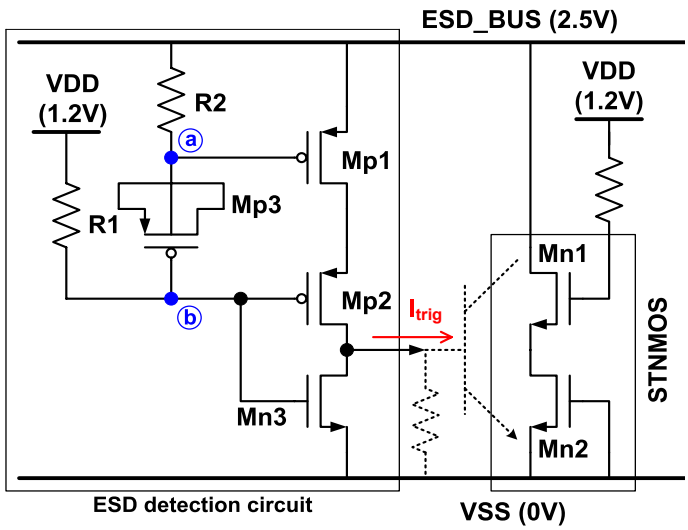


Figure 29.7.2: The new proposed high-voltage-tolerant power-rail ESD clamp circuit designed with only 1.2V devices for operating with ESD_BUS of 2.5V.

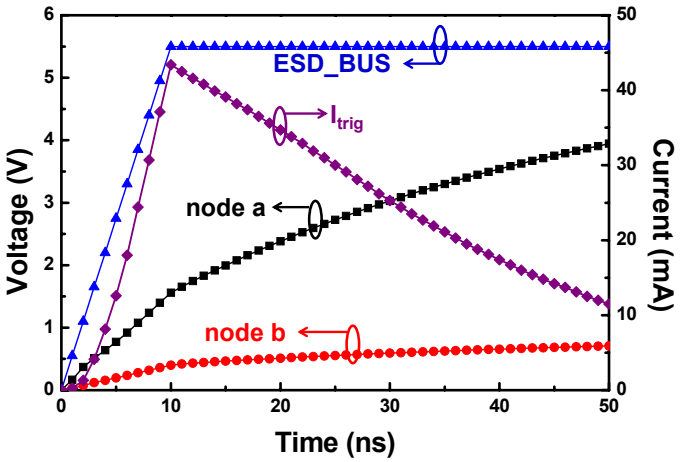
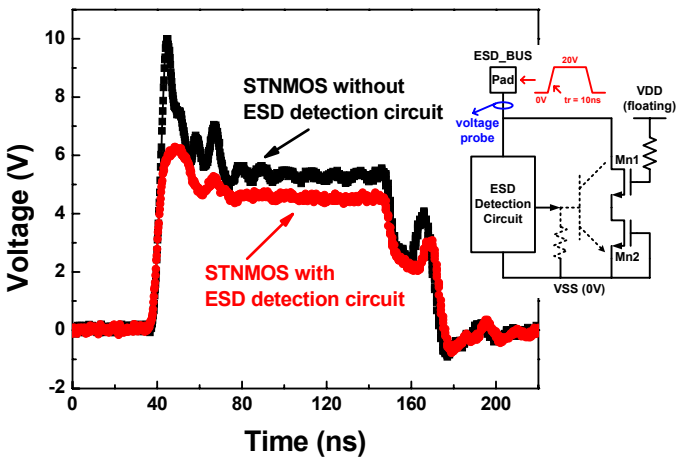


Figure 29.7.3: Hspice-simulated voltages on the nodes of ESD detection circuit and the trigger current (I_{trig}) through Mp2 in the high-voltage-tolerant power-rail ESD clamp circuit under 0-to-5.5V ESD-like transition.



29.7.4: Measured voltage waveforms to verify the turn-on efficiency of the high-voltage-tolerant power-rail ESD clamp circuit with STNMOS.

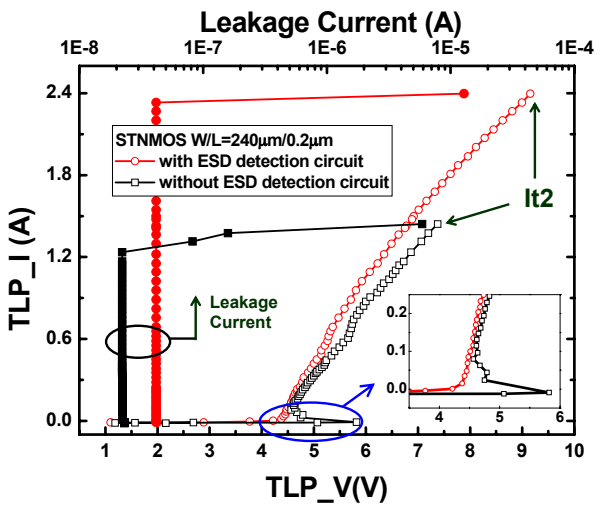


Figure 29.7.5: TLP-measured I-V curves of STNMOS with or without ESD detection circuit.

STNMOS W/L (μm/μm)	HBM ESD Level (kV)		MM ESD Level (V)	
	without detection circuit	with detection circuit	without detection circuit	with detection circuit
240/0.2	3	4	175	225
360/0.2	4	5	250	300
480/0.2	5	6.5	275	400

Figure 29.7.6: HBM and MM ESD levels of the STNMOS devices under different device dimensions with or without the ESD detection circuit.